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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/698,717	10/31/2003	Krzysztof Nauka	200310817-1	1558		
22879	7590 02/07/2006		EXAM	EXAMINER		
	PACKARD COMPAN	PHAM, VAN T				
P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			ART UNIT	PAPER NUMBER		
			2656			

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/698,717	NAUKA ET AL.				
Office Action Summary	Examiner	Art Unit				
	VAN T. PHAM	2656				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1)⊠ Responsive to communication(s) filed on <u>23 November 2005</u> .						
2a)⊠ This action is FINAL . 2b)☐ This						
·	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ☐ Claim(s) 1-12 and 21-29 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-12 and 21-29 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) ☐ The specification is objected to by the Examiner. 10) ☑ The drawing(s) filed on 31 October 2003 is/are: a) ☑ accepted or b) ☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal F 6) Other:					

Response to Arguments

1. Applicant's arguments filed 12/11/2005 have been fully considered.

Applicant's arguments with respect to claims 1-12, 21, 27-29 have been considered but are most in view of the new ground(s) of rejection.

Applicant's argument with respect to claim 22 has been fully considered but they are not persuasive.

In response to applicant's arguments, the recitation "A method of writing information to a layer of poled ferroelectric material" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 3. Claims 1-4, 6 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kasanuki et al. (US 5,481,527).

Regarding claim 1, Kasanuki discloses a data storage device comprising: a conductive probe having a tip (see Fig. 1, elements 1-2); a substrate including a semiconductor portion (see Fig. 1, element 4 and col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), the ferroelectric layer on the substrate (see Fig. 1, element 3-4), between the tip and the substrate (see Fig. 1, elements tip 1 and substrate 4), the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57- col.8, line 21).

Regarding claim 2, see col. 7, lines 29-36, discloses the device of claim 1, wherein the ferroelectric material includes a ferroelectric polymer.

Regarding claim 3, see col. 7, lines 29-36, discloses the ferroelectric material includes at least one of PVDF and PtrFE.

Regarding claim 4, see col. 7, lines 29-36, discloses the ferroelectric material includes an inorganic material (note: PbTiO3, Bi4Ti3O12, BaTiO3, LiNbO3,, PLZT).

Regarding claim 6, see col. 7, lines 29-36, discloses the device of claim 1, wherein electrical dipoles in the ferroelectric layer are oriented in a reference direction; the device further comprising a circuit for causing the probe to write to spaced-apart volumes on the ferroelectric layer, dipoles in the spaced apart volumes oriented in the reference direction to store a first logic value, and a different direction to store a second logic value (see Fig. 2, and col. 8, lines 5-21).

Regarding claim 9, discloses the device of claim 1, further comprising a circuit for causing the conductive probe to perform block and bulk erasure operations (see col. 10, lines 53-

causing the conductive probe to perform block and but
$$61)$$
: L $CM \cdot 3$ $line 52 - 53$.

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Regarding claim 10, discloses the device of claim 1, further comprising means for

heating the ferroelectric material above its Curie temperature, whereby block and bulk erasure

can be performed (note that Curie is an unit of radioactivity, see col. 8, line 45 - col. 9, line 18

and col.10, lines 53-61). & col. 3 lines 52-58.

4. Claims 22, and 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Gibson

(US 20020110074).

Regarding claim 22, see Figs. 1-5, discloses a method of writing information to a layer of

poled ferroelectric material, the method comprising using a probe to create local polarization

changes in the material, the probe having a tip diameter no more than several nanometers (see

col. 5, [0004], [0019], [0062] and [0065], [0070] note that by using the tip to write information

on the particles which particles size is around 10 nanometers; therefore the tip size is no more

than several nanometers).

Regarding claim 24, see Figs. 1-5, discloses the method of claim 22, wherein the probe is

used to write to spaced apart locations on the ferroelectric layer such that the spaced apart

locations have the same electrical dipole alignment as the rest of the ferroelectric layer, whereby

information at the spaced apart locations is erased (see [0015]-[0017], [0022], and [0071]-

[0072]).

Regarding claim 25, discloses the method of claim 22, further comprising heating the

ferroelectric layer above its Curie temperature, whereby block erasure of the ferroelectric layer is

performed (see Fig. 1-5, and col. 2, [0022]).

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Regarding claim 26, discloses the method of claim 22, further comprising heating selected areas of the ferroelectric layer above the Curie temperature of the ferroelectric layer, whereby the areas of the ferroelectric layer are erased (see Fig. 1-5, and col. 2, [0014], [0022]).

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 1, 5, 7-8, 11-12, 21 and 27-29 are rejected under 35 U.S.C. 103(a) as being anticipated by Cho (US 2003/0053400) In view of Kasanuki et al. (US 5,481,527).

Regarding claim 1, see Fig. 2, Cho discloses a data storage device comprising: a conductive probe having a tip (see Fig. 2, probe 14, and col. 1, [0012]); a substrate (see Fig. 2, element 12); and a data storage medium including a layer of poled ferroelectric material, the ferroelectric layer on the substrate, between the tip and the substrate (see Fig. 2, elements 11-13 and col. 4, [0049]). However, Cho does not disclose a substrate including a semiconductor portion, or the semiconductor portion and the ferroelectric layer forming an electrical junction.

Kasanuki discloses a data storage device comprising: a substrate including a semiconductor portion (see Fig. 1, element 4 and col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), and the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57- col.8, line 21).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide a substrate including a semiconductor portion and the semiconductor portion and the ferroelectric layer forming an electrical junction in Cho as suggested by Kasanuki, the motivation being in order for the surface of the electrode (or substrate) be not warped or strained (see Kasanuki col. 7, lines 27-28).

Regarding claim 5, the combination of Cho and Kasaniki, see Cho Figs. 1-2, discloses the device of claim 1, wherein the probe tip is no more than about 100 nanometers in diameter (see col. 1, [0005]).

Regarding claim 7, the combination of Cho and Kasaniki, see Cho Figs. 1-5, discloses the device of claim 1, further comprising a protective layer covering the ferroelectric layer, the protective layer not interfering with interactions between the probe tip and the ferroelectric layer (see Fig. 9, elements 81-83 and [0152]).

Regarding claim 8, the combination of Cho and Kasaniki, see Cho Figs. 1 and 2, discloses the device of claim 1, further comprising a circuit for causing the conductive probe to apply local electric fields to the ferroelectric layer during write operations, the local electric fields causing local polarization changes in the ferroelectric material (see abstract, col. 5, [0071]).

Regarding claim 11, the combination of Cho and Kasaniki, see Cho Figs. 1-5, discloses the device of claim 1, further comprising a read circuit for using the probe to sense changes in capacitance or leakage current of the junction (see Fig. 1, elements Csa, Csb,...Csn and [0071]-[0075]).

Regarding claim 12, the combination of Cho and Kasaniki, see Cho Figs. 1-2 and abstract, discloses the device of claim 1, further comprising a read circuit for using the probe to apply an ac signal to local areas on the ferroelectric material, and detect changes in a non-linear component of a dielectric constant (see Cho col. 1, [0070]-[0075]).

Regarding claim 21, see rejection above of claim 1, the combination of Cho and Kasanuki, further see Cho Figs. 1-2, discloses a plurality of sharp-tip probes (see col. 5, [0073]); means for causing the probes to create local polarization changes in the ferroelectric layer during write operations; and means for using the probes to detect polarization of local areas on the ferroelectric layer during read operations (see col.4, [0071]-[0075]).

Regarding claim 27, see rejection above of claims 1 and 22, the combination of Cho and Kasanuki, further see Figs. 1-5, discloses a method of using the probe and the semiconductor to detect polarity reversal at designated locations on the ferroelectric layer, each polarity reversal at a designated location indicating a first stored value at that designated location, each non-reversal of polarity at an expected location indicating a second logic value stored at that designated location (see Figs. 1-2, abstract and col. 5, [0070]-[0075]).

Regarding claim 28, see rejection above of claim 11.

Regarding claim 29, see rejection above of claim 12.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson (US 20020110074) in view of Thomas (US 6,046,973).

Regarding claim 23, Gibson, according to Figs. 15, discloses the device of claim 22, wherein the ferroelectric layer has electrical dipole (see col. 6, [0071]-[0072]) and discloses the

probe can write information to the recording medium. However, Gibson does not disclose the direction of dipole in the ferroelectric layer.

Thomas, see Fig. 1, discloses electrical dipoles in the ferroelectric layer are oriented in a reference direction; the device further comprising a circuit for causing the probe to write to spaced-apart volumes on the ferroelectric layer, dipoles in the spaced apart volumes oriented in the reference direction to store a first logic value, and a different direction to store a second logic value (see abstract and col. 2, lines 1-48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide an electrical dipoles in the ferroelectric layer with vary directions in Gibson as suggested by Thomas, the motivation being in order to change the positive or negative polarization potential difference of a ferroelectric molecule in the media (see Thomas col. 2, lines 7-8).

Cited References

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The cited references relate to information processing apparatus with ferroelectric rewritable recording medium and methods for conducting between a scanned-probe and storage medium.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VAN T. PHAM whose telephone number is 571-272-7590. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

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supervisor, HOA T. NGUYEN can be reached on 571-272-7579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VP.

PRIMARY EXAMINER

floa Nguyen (SPE) 2656.